REMARKS

Claims 1-28 are pending. By this Amendment, editorial changes are made to the specification.

Applicant appreciates the Examiner's allowance of claims 1-16. Claims 17-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Reblewski et al. U.S. Patent No. 6,265,894 in view of Reblewski U.S. Patent No. 6,473,726. This rejection is respectfully traversed. As explained below, neither reference qualifies as prior art, and in any event the asserted reference combination does not teach or suggest the inventions of the rejected claims.

The Reblewski '726 patent and the present application are of common (identical) inventorship. In view of the common inventorship and the fact that the '726 patent did not issue until well after the filing date of the present application, the '726 patent does not qualify as prior art under any section of 35 U.S.C. § 102. Moreover, the Reblewski et al. '894 patent is disqualified as prior art under 35 U.S.C. § 103(c), in that the inventions of the present application and the '894 Reblewski et al. patent were, at the time the present invention was made, owned by or subject to an obligation of Assignment to the same person (entity). See MPEP § 706.02(I)(2).

The asserted combination does not teach or suggest the present inventions of rejected claims 17-28 in any event. In the combination asserted in the Office Action, it is proposed to modify the teaching of Reblewski et al. '894 to include a partitioner as taught by Reblewski et al. '726. Such a combination would not result in any of the claimed inventions. The system of the '894 patent permits a dynamic reconfiguration of an integrated circuit which allows a partial scan register to capture and output the states of otherwise hidden nodes. This does not teach or suggest the present inventions, which correspondingly and distributively (claims 17 and 21), or locally (claims 23 and 27), generate configuration signals to configure selected ones of

reconfigurable logic and interconnect resources to emulate circuit elements of corresponding partitions of an IC design. Rather than providing distributed or local reconfiguration of logic and interconnect resources to emulate circuit elements, the dynamic reconfiguration of Reblewski et al. '894 serves to permit access to hidden notes. As shown in Fig. 10 of the '894 patent (referenced by the Examiner), it is a central host system with circuit design mapping software that is used to configure the logic and interconnect resources of Reblewski et al. '894 to emulate circuit elements, not distributed or local resources.

For all of the foregoing reasons, it is respectfully submitted that the rejections of claims 17-28 should be withdrawn. Should the Examiner believe that anything further is desirable in order to place the application in condition for allowance, he is respectfully urged to telephone applicant's undersigned representative at the below-listed number.

Respectfully submitted,

Christopher L. McKee
Registration No. 32,384

BANNER & WITCOFF, LTD.
1001 G Street, N.W., 11th Floor
Washington, D.C. 20001-4597
(202) 824-3000

Date: June 7, 2005

C:\NrPortbl\IMAN_WDC\BSAMUELS\864700_1.DOC